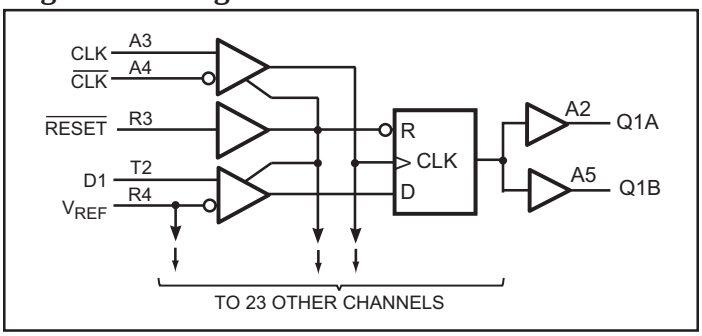
24-Bit to 48-Bit Registered Buffer

Product Features

- PI74 SSTVF32852A is designed for low-voltage operation, 2.5V for PC1600 ~ PC2700; 2.6V for PC3200
- Supports SSTL_2 Class I specifications on outputs
- All Inputs are SSTL_2 Compatible, except $\overline{\text{RESET}}$ which is LVCMOS.
- Designed for DDR Memory
- Packaging: 114-Ball LFBGA
  - Pb-free available

Logic Block Diagram



Product Pin Description

Pin Name	Description
$\overline{\text{RESET}}$	Reset (Active Low) LVCMOS
CLK	Clock Input, Positive Differential Input
$\overline{\text{CLK}}$	Clock Input, Negative Differential Input
D	Data Input
Q	Data Output
GND	Ground
V_{DD}	Core Supply Voltage, 2.5V Nominal
V_{DDQ}	Output Supply Voltage, 2.5V Nominal
V_{REF}	Input Reference Voltage, 1.25V Nominal

Product Description

Pericom Semiconductor's PI74SSTVF32852A logic circuit is produced using the Company's advanced sub-micron CMOS technology, achieving industry leading speed.

All inputs are compatible with the JEDEC standard for SSTL_2, except the LVCMOS reset ($\overline{\text{RESET}}$) input. All outputs are SSTL_2, Class II compatible.

The device operates from a differential clock (CK and $\overline{\text{CK}}$). Data registered at the crossing of CK going HIGH, and $\overline{\text{CK}}$ going LOW.

The PI74SSTVF32852A supports low-power standby operation. When $\overline{\text{RESET}}$ is LOW, the differential input receivers are disabled, and undriven (floating) data, clock and reference voltage (VREF) inputs are allowed. In addition, when $\overline{\text{RESET}}$ is LOW, all registers are reset, and all outputs are forced LOW. The LVCMOS $\overline{\text{RESET}}$ input must always be held at a valid logic HIGH or LOW level.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{\text{RESET}}$ must be held in the LOW state during power up.

In the DDR DIMM application, $\overline{\text{RESET}}$ is specified to be completely asynchronous with respect to CK and $\overline{\text{CK}}$. Therefore, no timing relationship can be guaranteed between the two. When entering $\overline{\text{RESET}}$, the register will be cleared and the outputs will be driven LOW quickly, relative to the time to disable the differential input receivers, thus ensuring no glitches on the output. However, when coming out of $\overline{\text{RESET}}$, the register will become active quickly, relative to the time to enable the differential input receivers. When the data inputs are LOW, and the clock is stable, during the time from the LOW-to-HIGH transition of $\overline{\text{RESET}}$ until the input receivers are fully enabled, the design must ensure that the outputs will remain LOW.

Pericom's PI74SSTVF32852A is characterized for operation from 0° to 70°C.

Truth Table[1]

Inputs				Outputs
$\overline{\text{RESET}}$	CLK	$\overline{\text{CLK}}$	D	Q
L	X or Floating	X or Floating	X or Floating	L
H	↑	↓	H	H
H	↑	↓	L	L
H	L or H	L or H	X	Qo[2]

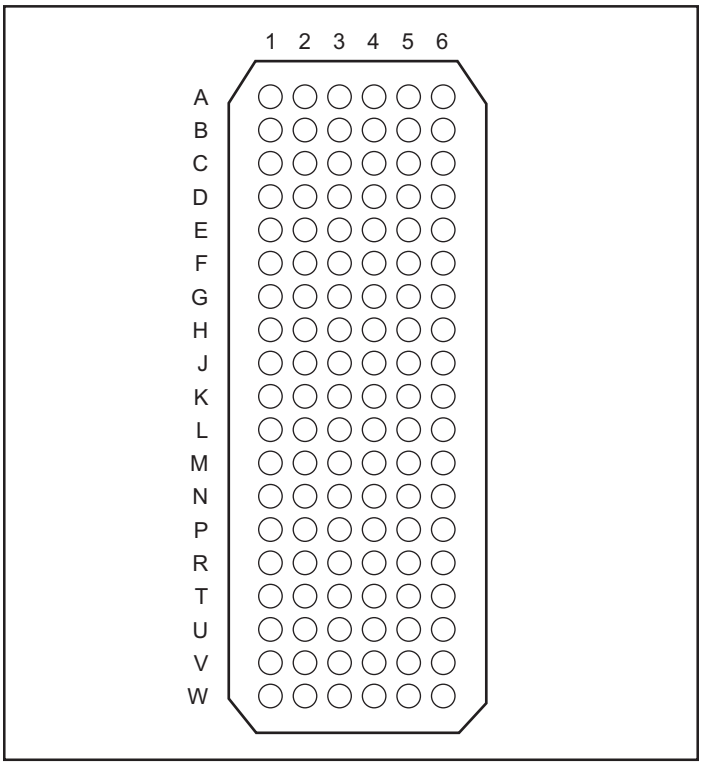
Notes:

1. H = High Signal Level; L = Low Signal Level; ↑ = Transition LOW-to-HIGH; ↓ = Transition HIGH-to-LOW
   X = Irrelevant or floating
2. Output level before the indicated steady state input conditions were established.

Product Pin Configuration

	1	2	3	4	5	6
A	Q2A	Q1A	CLK	$\overline{CLK}$	Q1B	Q2B
B	Q3A	V_{DDQ}	GND	GND	V_{DDQ}	Q3B
C	Q5A	Q4A	V_{DDQ}	V_{DDQ}	Q4B	Q5B
D	Q7A	Q6A	GND	GND	Q6B	Q7B
E	Q8A	GND	V_{DDQ}	V_{DDQ}	GND	Q8B
F	Q10A	Q9A	V_{DDQ}	V_{DDQ}	Q9B	Q10B
G	Q12A	Q11A	GND	GND	Q11B	Q12B
H	Q13A	V_{CC}	V_{DDQ}	V_{DDQ}	V_{CC}	Q13B
J	Q14A	Q15A	GND	GND	Q15B	Q14B
K	Q17A	Q16A	V_{DDQ}	V_{DDQ}	Q16B	Q17B
L	Q18A	Q19A	GND	GND	Q19B	Q18B
M	Q20A	V_{DDQ}	GND	GND	V_{DDQ}	Q20B
N	Q22A	Q21A	V_{DDQ}	V_{DDQ}	Q21B	Q22B
P	Q23A	V_{DDQ}	GND	GND	V_{DDQ}	Q23B
R	Q24A	V_{CC}	$\overline{RESET}$	V_{REF}	V_{CC}	Q24B
T	D2	D1	D6	D18	D13	D14
U	D4	D3	D10	D22	D15	D16
V	D5	D7	D11	D23	D19	D17
W	D8	D9	D12	D24	D21	D20

NB Package (Top View)



Maximum Ratings (Above which the useful life may be impaired. For user guidelines, not tested.)

Item	Symbol/Conditions	Ratings	Units
Storage temperature	T_{stg}	–65 to 150	°C
Supply voltage	V_{DD} or V_{DDQ}	–0.5 to 3.6	V
Input voltage(1,2)	V_I	–0.5 to V_{DD} +0.5	
Output voltage(1,2)	V_O	–0.5 to V_{DDQ} +0.5	
Input clamp current	I_{IK}, V_I <0 or V_I >V_{DD}	–50	mA
Output clamp current	I_{OK}, V_O <0 or V_O >V_{DDQ}	±50	
Continuous output current	I_O, V_O = 0 to V_{DDQ}	±50	
V_{DD}, V_{DDQ} or GND current/pin	I_{DD}, I_{DDQ} or I_{GND}	±100	
Package Thermal Impedance(3)	θJ_A	36	°C/W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

1. The input and output negative voltage ratings may be excluded if the input and output clamp ratings are observed.
2. This value is limited to 3.6V Maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions(4)

Parameters	Description		Min.	Nom.	Max.	Units
V_{DD}/V_{DDQ}	Core Output Supply Voltage	PC1600 PC2700	2.3	2.5	2.7	V
		PC3200	2.5	2.6	2.7	
V_{REF}	Reference Voltage V_{REF} = 0.5X V_{DDQ}	PC1600 PC2700	1.15	1.25	1.35	
		PC3200	1.25	1.3	1.35	
V_{TT}	Termination Voltage		V_{REF} –0.04	V_{REF}	V_{REF} +0.04	
V_I	Input Voltage		0		V_{DD}	
V_{IH}	AC High -Level Input Voltage	Data Inputs	V_{REF} +310mV			
V_{IL}	AC Low -Level Input Voltage				V_{REF} – 310mV	
V_{IH}	DC High -Level Input Voltage		V_{REF} +150mV			
V_{IL}	DC Low -Level Input Voltage				V_{REF} –150mV	
V_{IH}	High -Level Input Voltage	$\overline{\text{Reset}}$	1.7			
V_{IL}	Low -Level Input Voltage				0.7	
V_{ICR}	Common-mode input range	CK, $\overline{\text{CK}}$	0.97		1.53	
V_{ID}	Differential Input Voltage		360			
I_{OH}	High-Level Output Current				–16	mA
I_{OL}	Low-Level Output Current				16	
T_A	Operating Free-Air Temperature		0		70	°C

Note:
4. The $\overline{\text{RESET}}$ input of the device must be held at V_{DD} or GND to ensure proper device operation. The differential inputs must not be floating, unless $\overline{\text{RESET}}$ is LOW.

DC Electrical Characteristics for PC1600 ~ PC2700

(Over the Operating Range, $T_A = 0°C$ to $+70°C$, $V_{DD} = 2.5V \pm 200mV$, $V_{DDQ} = 2.5V \pm 200mV$)

Parameters		Test Conditions		Vcc	Min.	Typ.(1)	Max.	Units
V_{IK}		$I_I = -18mA$		2.3V			–1.2	V
V_{OH}		$I_{OH} = -100\mu A$		2.3V-2.7V	$V_{DD} - 0.2V$			
		$I_{OH} = -8mA$		2.3V	1.95			
V_{OL}		$I_{OL} = 100\mu A$		2.3V-2.7V			0.2	
		$I_{OH} = 8mA$		2.3V			0.35	
I_I	All Inputs,	$V_I = V_{DD}$ or GND		2.7V			±5	µA
I_{DD}	Standby (Static)	$\overline{RESET}$ = GND	$I_O = 0$	2.7V			10	µA
	Operating Static	$\overline{RESET} = V_{DD}$ $V_I = V_{IH}$ (AC) or V_I (AC)					35	mA
I_{DDD}	Dynamic Operating - Clock only	$\overline{RESET} = V_{DD}$ $V_I = V_{IH}$(AC) or V_{IL}(AC), CK and $\overline{CK}$ switching 50% duty cycle				46		µA/ clock MHz
	Dynamic Operating -per each data input	$\overline{RESET} = V_{DD}$ $V_I = V_{IH\ (AC)}$ or $V_{IL(AC)}$, CK and $\overline{CK}$ switching 50% duty cycle. One data input switching at half clock frequency, 50% duty cycle				12		µA/ clock MHz Data
C_I	Data inputs	$V_I = V_{REF} \pm 310mV$		2.5V	3.0	4.0	5.5	pF
	CK and $\overline{CK}$	V_{ICR}= 1.25V, $V_{I(PP)}$ = 360mV			6.5	8.0	9.5	
	$\overline{RESET}$	$V_I = V_{CC}$ or GND			3.5	4.35	5.0	

Note:

1. All typical values are at $V_{DD} = 2.5V$, $T_A = 25°C$.

DC Electrical Characteristics for PC3200

(Over the Operating Range, $T_A = 0°C$ to $+70°C$, $V_{DD} = 2.6V \pm 100mV$, $V_{DDQ} = 2.6V \pm 100mV$)

Parameters		Test Conditions		Vcc	Min.	Typ.(1)	Max.	Units
V_{IK}		$I_I = -18mA$		2.5V			–1.2	V
V_{OH}		$I_{OH} = -100\mu A$		2.5V-2.7V	$V_{DD} - 0.2V$			
		$I_{OH} = -8mA$		2.5V	1.95			
V_{OL}		$I_{OL} = 100\mu A$		2.5V-2.7V			0.2	
		$I_{OH} = 8mA$		2.5V			0.35	
I_I	All Inputs,	$V_I = V_{DD}$ or GND		2.7V			±5	µA
I_{DD}	Standby (Static)	$\overline{RESET}$ = GND	$I_O = 0$	2.7V			10	µA
	Operating Static	$\overline{RESET} = V_{DD}$ $V_I = V_{IH}$ (AC) or V_I (AC)					35	mA
I_{DDD}	Dynamic Operating - Clock only	$\overline{RESET} = V_{DD}$ $V_I = V_{IH}$(AC) or V_{IL}(AC), CK and $\overline{CK}$ switching 50% duty cycle				46		µA/ clock MHz
	Dynamic Operating -per each data input	$\overline{RESET} = V_{DD}$ $V_I = V_{IH\ (AC)}$ or $V_{IL(AC)}$, CK and $\overline{CK}$ switching 50% duty cycle. One data input switching at half clock frequency, 50% duty cycle				12		µA/ clock MHz Data
C_I	Data inputs	$V_I = V_{REF} \pm 350mV$		2.6V	3.0	4.0	5.5	pF
	CK and $\overline{CK}$	V_{ICR}= 1.25V, $V_{I(PP)}$ = 360mV			6.5	8.0	9.5	
	$\overline{RESET}$	$V_I = V_{CC}$ or GND			3.5	4.35	5.0	

Note:

1. All typical values are at $V_{DD} = 2.5V$, $T_A = 25°C$.

Timing Requirements (over recommended operating free-air temperature range, unless otherwise noted)

			V_{DD}=2.5V ±0.2V		V_{DD}=2.6V ±0.1V		Units
			Min.	Max.	Min.	Max.	
fclock	Clock Frequency			270		270	MHz
t_W	Pulse Duration, CLK, $\overline{CLK}$ High or Low		2.5		2.5		ns
t_{act}	Differential inputs active time, data inputs must be low after $\overline{RESET}$ High		22		22		
t_{inact}	Differential Inputs inactive time, data and clock inputs must be held at valid levels (not floating) after $\overline{RESET}$ Low		22		22		
t_{SU}	Setup time, fast slew rate (5,7)	Data before CK↑ ,$\overline{CK}$↓	0.75		0.75		
	Setup time, slow slew rate (6,7)		0.9		0.9		
t_h	Hold time, fast slew rate (5,7)	Data before CK↑ ,$\overline{CK}$↓	0.75		0.75		
	Hold time, slow slew rate (6,7)		0.9		0.9		

Notes:
5. Data signal input slew rate ≥ 1 V/ns
6. Data signal input slew rate ≥ 0.5V/ns and <1V/ns
7. CLK, $\overline{CLK}$ input slew rates are ≥ 1 V/ns.

Switching Characteristics for PC1600~PC2700

(over recommended operating free-air temperature range, unless otherwise noted.)
(See test circuits and switching waveforms).

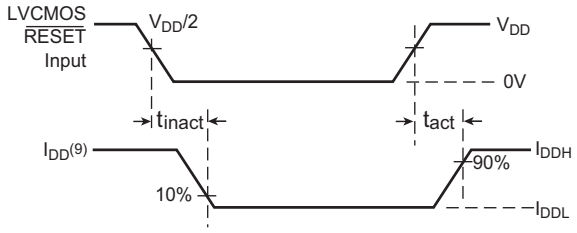
Parameter	From (Input)	To (Output)	V_{DD} = 2.5V ±0.2V			Units
			Min.	Typ.	Max.	
f_{max}			210			MHz
t_{pd}	CLK, $\overline{CLK}$	Q	1.1		2.1	ns
t_{phl}	$\overline{RESET}$	Q			5.0	

Switching Characteristics for PC3200

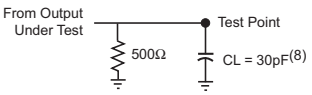
(over recommended operating free-air temperature range, unless otherwise noted.)
(See test circuits and switching waveforms).

Parameter	From (Input)	To (Output)	V_{DD} = 2.6V ±0.1V			Units
			Min.	Typ.	Max.	
f_{max}			210			MHz
t_{pd}	CLK, $\overline{CLK}$	Q	1.1		2.1	ns
t_{phl}	$\overline{RESET}$	Q			5.0	

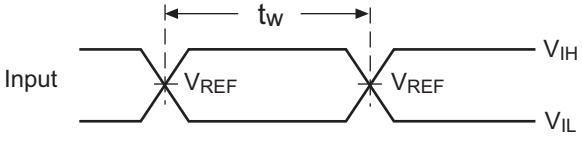
Test Circuit and Switching Waveforms



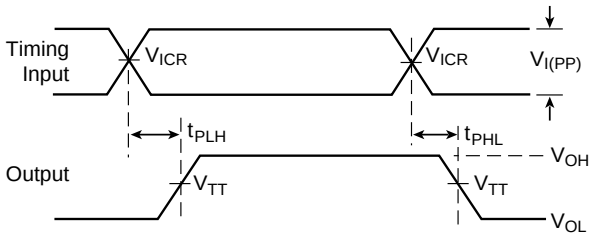
Voltage and Current Waveforms
Input Active and Inactive Times



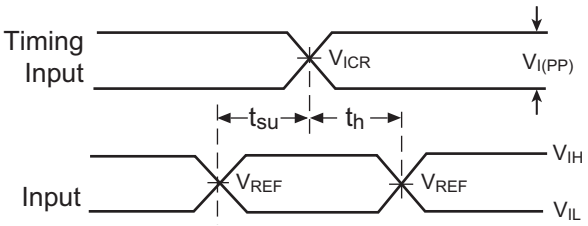
Load Circuit



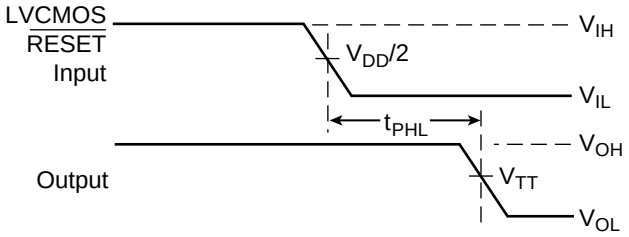
Voltage Waveforms - Pulse Duration



Voltage Waveforms - Propagation Delay Times



Voltage Waveforms - Setup and Hold Times



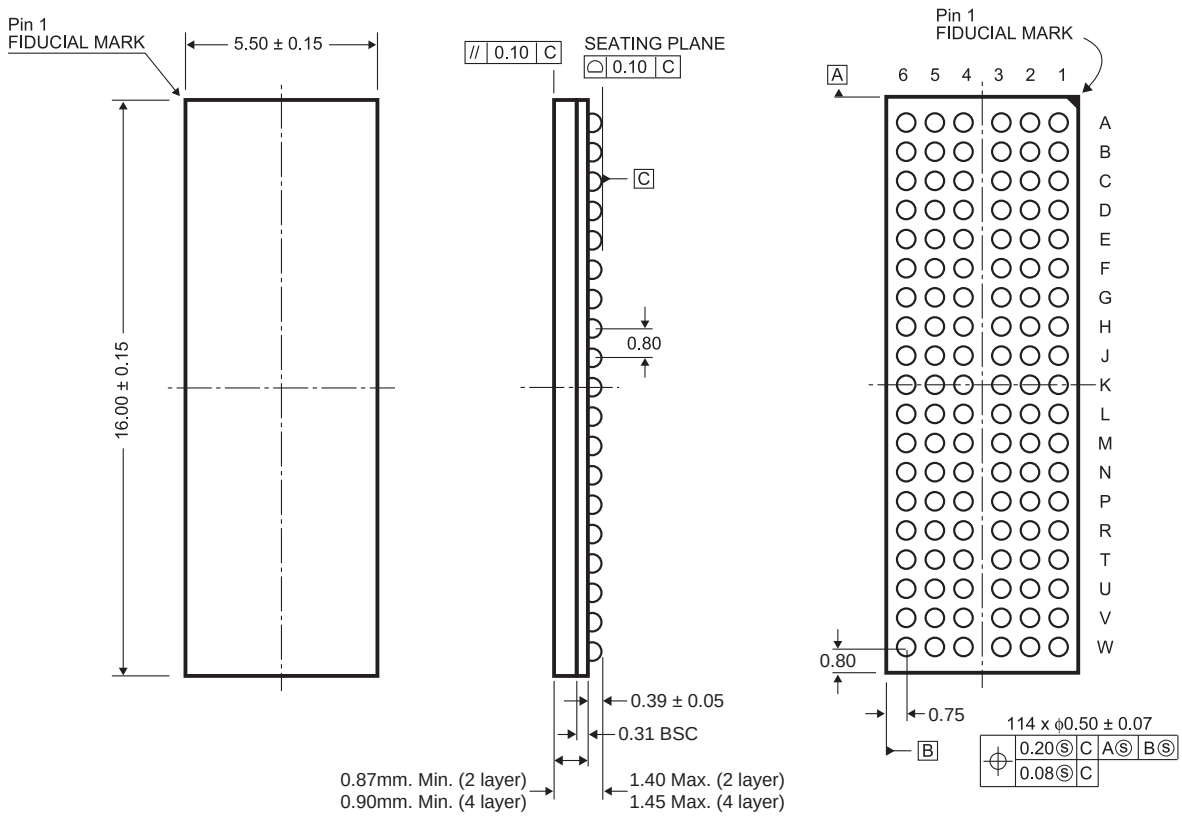
Voltage Waveforms - Propagation Delay Times

Parameter Measurement Information

Notes:

8. C_L includes probe and jig capacitance.
9. I_{DD} tested with clock and data inputs held at V_{DD} or GND, and I_O = 0mA.
10. All input pulses are supplied by generators having the following characteristics: PRR ≤10 MHz, Z_O = 50 ohms. Input slew rate = 1V/ns ±20% (unless otherwise specified).
11. The outputs are measured one at a time with one transition per measurement.
12. $V_{TT} = V_{REF} = V_{DDQ}/2$
13. $V_{IH} = V_{REF} + 310mV$ (ac voltage levels) for SSTL inputs. $V_{IH} = V_{DD}$ for LVCMOS input.
14. $V_{IL} = V_{REF} + 310mV$ (ac voltage levels) for SSTL inputs. V_{IL} = GND for LVCMOS input.
15. t_{PLH} and t_{PHL} are the same as t_{pd}.

114-Ball LFBGA (NB) Package



Ordering Information

Ordering Code	Package Code	Package Type
PI74SSTVF32852ANB	NB	114-Ball LFBGA

Notes:
1. Thermal characteristics can be found on the company web site at http://www.pericom.com/packaging/mechanicals.php